Offset Reduction Techniques in Highspeed Analog-To-Digital Converters [Analysis, Design and Tradeoffs /

Figueiredo, Pedro M.

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Monografía

Offset Reduction Techniques in High-Speed Analog-to-Digital Converters analyzes, describes the design, and presents test results of Analog-to-Digital Converters (ADCs) employing the three main high-speed architectures: flash, two-step flash and folding and interpolation. The advantages and limitations of each one are reviewed, and the techniques employed to improve their performance are discussed. Since the offset voltages of the constituting sub-blocks of these converters (pre-amplifiers, folding circuits and latched comparators) present the definitive linearity limitation, the offset is the fundamental design parameter in high-speed CMOS ADCs. Consequently, offset reduction techniques must be employed, in order to achieve high frequency operation with low power and layout area. Averaging and offset sampling are the most widely used, both being thoroughly characterized: the most exhaustive study ever performed about averaging in both pre-amplifier and folding stages is presented, covering the DC and transient responses, all mismatch sources, termination, and a fully automated design procedure; existing offset sampling methods are carefully reviewed, and two new techniques are disclosed that, combined, yield a (nearly) offset free comparator. Other relevant topics include kickback noise elimination in comparators, reference buffer design, a technique to compensate (certain) IR drops, details on the layout and floorplan of cascaded folding stages, and an improved scheme to select reference voltages in fine ADCs of two-step subranging converters. Special emphasis is given to the methods of guaranteeing specifications across process, temperature and supply voltage corners

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