



Substrate Noise Coupling in RFICs [

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Monografía

Substrate Noise Coupling in RFICs addresses substrate noise coupling in RF and mixed signal ICs when used in a system on chip (SoC) containing digital ICs as well. This trend of integrating RF, mixed signal ICs with large digital ICs is found in many of today's commercial ICs such as single chip Wi-Fi or Bluetooth solutions and is expected to grow rapidly in the future. The book reports modeling and simulation techniques for substrate noise coupling effects in RFICs and introduces isolation structures and design guides to mitigate such effects with the ultimate goal of enhancing the yield of RF and mixed signal SoCs. This is particularly critical when process feature sizes scale down to the nano meter range. Substrate Noise Coupling in RFICs reports silicon measurements, new test and noise isolation structures as well as calibration of a design flow used in the design and debug phases of RFICs. A design guide is articulated to be used by RFIC designers to maximize signal isolation and optimize chip floor plan, power and ground domains. Industrial examples of RFICs are given as demonstration vehicles to validate the proposed techniques. Some emphasis is put on the design of on-chip spiral inductors and the impact of the substrate on their performance. To our knowledge, this is the first title devoted to the topic of substrate noise coupling in RFICs as part of a large SoC

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