

Rapid prototyping of digital systems : a tutorial approach /

Hamblen, James O. (1954-)

Kluwer Academic, 2002

Electronic books

Monografía

Rapid Prototyping of Digital Systems, Second Edition provides an exciting and challenging laboratory component for an undergraduate digital logic design class. The more advanced topics and exercises are also appropriate for consideration at schools that have an upper level course in digital logic or programmable logic. Design engineers working in industry will also want to consider this book for a rapid introduction to FPLD technology and logic synthesis using commercial CAD tools, especially if they have not had previous experience with the new and rapidly evolving technology. Two tutorials on the Altera CAD tool environment, an overview of programmable logic, and a design library with several easy-to-use input and output functions were developed for this book to help the reader get started quickly. Early design examples use schematic capture and library components. VHDL is used for more complex designs after a short introduction to VHDL-based synthesis. A coupon is included with the text for purchase of the new UP 1X board. The additional logic and memory in the UP 1X's FLEX 10K70 is useful on larger design projects such as computers and video games. The second edition includes an update chapter on programmable logic, new robot sensors and projects, optional Verilog examples, and a meta assembler which can be used to develop assemble language programs for the computer designs in Chapters 8 and 13

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Título: Rapid prototyping of digital systems a tutorial approach James O. Hamblen, Michael D. Furman

Edición: 2nd ed

Editorial: Boston Kluwer Academic 2002

Descripción física: 1 online resource (xvi, 288 pages) illustrations

Nota general: Includes index

Contenido: Tutorial I: The 15 Minute Design -- Design Entry using the Graphic Editor -- Compiling the Design --Simulation of the Design -- Downloading Your Design to the UP 1 or UP 1X Board -- The 10 Minute VHDL Entry Tutorial -- Compiling the VHDL Design -- The 10 Minute Verilog Entry Tutorial -- Compiling the Verilog Design -- Timing Analysis -- The Floorplan Editor -- Symbols and Hierarchy -- Functional Simulation -- The Altera UP 1 and UP 1X CPLD Boards -- Programming Jumpers -- MAX 7000 Device and UP 1 I/O Features -- MAX and FLEX Seven-segment LED Displays -- FLEX 10K Device and UP 1 I/O Features -- Obtaining a UP 1 or UP 1X Board and Power Supply -- Programmable Logic Technology -- CPLDs and FPGAs -- Altera MAX 7000S Architecture -- A Product Term CPLD Device -- Altera FLEX 10K Architecture -- A Look-Up Table CPLD Device -- Xilinx 4000 Architecture -- A Look-Up Table FPGA Device -- Computer Aided Design Tools for Programmable Logic -- Next Generation FPLD CAD tools -- Applications of FPLDs -- Features of New Generation FPLDs --Tutorial II: Sequential Design and Hierarchy -- Install the Tutorial Files and UP1core Library -- Open the tutor2 Schematic -- Browse the Hierarchy -- Using Buses in a Schematic -- Testing the Pushbutton Counter and Displays -- Testing the Initial Design on the UP 1 Board -- Fixing the Switch Contact Bounce Problem -- Testing the Modified Design on the UP 1 Board -- UP1core Library Functions -- UP1core DEC_7SEG: Hex to Seven-segment Decoder -- UP1core Debounce: Pushbutton Debounce

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ISBN: 0306476355 eBook) 9780306476358 eBook) 0792374398 alk. paper) 9780792374398 alk. paper)

Materia: Dispositivos FPGAs- Computer-aided design Programmable array logic VHDL (Computer hardware description language) TECHNOLOGY & ENGINEERING- Electronics- Circuits- VLSI & ULSI. TECHNOLOGY & ENGINEERING- Electronics- Circuits- Logic. COMPUTERS- Logic Design. Programmable array logic. VHDL (Computer hardware description language)

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Enlace a formato físico adicional: Print version Hamblen, James O., 1954-. Rapid prototyping of digital systems. 2nd ed. Boston : Kluwer Academic, 2002 (DLC) 2001038307

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