Analog-baseband architectures and circuits for multistandard and low-voltage wireless transceive /

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Monografía

With the past few decade efforts on lithography and integrated-circuit (IC) technologies, very low-cost microsystems have been successfully developed for many different applications. The trend in wireless communications is toward creating a networkubiquitous era in the years to come. Many unprecedented opportunities and challenges, such as Design for multi-standardability and low-voltage (LV) compliance, are rapidly becoming the mainstream directions in wireless-IC research and development, given that the former can offer the best connectivity among different networks, while the latter can facilitate the technology migration into the sub-1-V nanoscale regimes for further cost and power reduction. Analog-Baseband Architecturees and Circuits presents architectural and circuit techniques for wireless transceivers to achieve multistandard and low-voltage compliance. The first part of the book reviews the physical layer specifications of modern wireless communication standards, presents the fundamental tradeoffs involved in transceiver architecture selection, and provides case studies of the state-of-the-art multistandard transceivers, where the key techniques reinforced are highlighted and discussed. A statistical summary (with 100+ references cited) of most used transmitter and receiver architectures for modern communication standards is provided. All the references are citied from the leading forums, i.e., ISSCC, CICC, VLSI and ESSCIRC, from 1997 to 2005. The second part focuses on the architectural design of multistandard transceivers. A coarse-RF fine-IF (two-step) channelselection technique is disclosed. It, through the reconfiguration of receiver and transmitter analog basebands, enables not only a relaxation of the RF frequency synthesizers and local oscillators design specifications, but also an efficient multistandard compliance by synthesizing the low-IF and zero-IF in the receiver; and the direct-up and two-step-up in the transmitter. The principle is d emonstrated in few design examples. One of them is a system-in-a-package (SiP) receiver analog baseband for IEEE 802.11a/b/g WLAN. It not only has the two-step channel selection embedded, but also features a flexible-IF topology, a unique 3D-stack floorplan, and a particular design methodology for high testability and routability. The third part deals with the circuit design. In addition to the methodical description of many LV circuit techniques, 3 tailormade LV-robust functional blocks are presented. They include: 1) a double-quadrature-downconversion filter (DQDF) - it realizes concurrently clock-rate-defined IF reception, I/Q demodulation, IF channel selection and baseband filtering. 2) A switched-current-resistor (SCR) programmable-gain amplifier (PGA) - it offers a transient-free constant-bandwidth gain

adjustment. 3) An inside-OpAmp dc-offset canceler - it saves the silicon area required for realizing a large time constant on chip while maximizing its highpass-pole switchability for fast dc-offset transient. The last part presents experimental results of the 3 tailor-made building blocks and a fully-integrated analog-baseband IC fabricated in a standard-VTH CMOS process. Previously untold on-/off-chip co-setup for both full-chip and building blocks measurements are described. Not only the building blocks have successfully extended the state-of-the-art boundary in terms of signal bandwidth and supply voltage, the analog-baseband IC has been so far the lowest-voltage-reported solution for IEEE 802.11a/b/g WLAN receivers

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