Full-Chip Nanometer Routing Techniques [

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Monografía

As Moore's Law continues unencumbered into the nanometer era, chips are reaching 1000 M gates in size, process geometries have shrunk to 90 nm and below, and engineers have to face compounded design complexity with every new design. These nanometer-scale designs require a new generation of physics-aware and manufacturing-aware routing. At 90 nm and below, there are so many signal-integrity issues that design teams cannot manually correct them all. At 90 nm, wires account for nearly 75% of the total delay in a circuit. Even more insidious, however, is that among nearly 40% of these nets, more than 50% of their total net capacitance are attributed to the cross-coupling capacitance between neighboring signals. At this point a new design and optimization paradigm based on real wires is required. Nanometer routers must prevent and correct these effects on-the-fly in order to reach timing closure. From a manufacturability standpoint, nanometer routers must explicitly deal with the ever increasing design complexity, and be capable of adapting to the constraint requirements of timing, signal integrity, process antenna effect, and new interconnect architecture such as X-architecture. In the nanometer era, we must look into new-generation routing technologies that combine high performance and capacity with the integration of congestion, timing, SI prevention, and DFM algorithms as the best means of getting to design closure quickly. In this book, we present a novel multilevel full-chip router, namely mSIGMA for SIGnal-integrity and MAnufacturability optimization. And these routing technologies will ensure faster time-to-market and time-to-profitability

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